Exhibit A

In the Specification:

The bottom and top of channel 204 may be defective. Particularly if the epitaxial layer is thin, the region is likely to be extremely small and may not be significant to the formation of the device. However, if it is necessary to remove [reove] these regions, two processes are available to do so at small but tolerable, degrade of device width control.[.] Specifically, a spacer could be deposited similar to that of spacer 302 of Figure 3B, but etched lower to uncover the top of the epitaxial region. After this spacer is formed, the buried oxide is etched underneath the spacer as shown on the left side of Figure 12. Alternatively, a thin composite spacer may be used. In this case, the bottom of the spacer are isotropicallly etched to uncover the top and bottom regions. The height of the spacer (overetch) is determined by the undercut necessary to reach the epitaxial region at the bottom of the spacer, as shown on the right side of Figure 12. After the defective regions are etched, the spacers are removed selectively to the epitaxial regions and the buried oxide layer before proceeding to following processing steps. It should be noted that it is also possible to perform the procedure described above after the spacer shown in Figure 4B is removed with the spacers of the above described procedure being removed before further processing.

In the Claims:

1. (Amended) A method of forming a field effect transistor (FET) transistor, comprising:

providing a substrate;

forming a layer on the substrate, the layer having a side surface;

forming an epitaxial channel on the side surface, the channel having a first sidewall;

removing the layer for exposing a second sidewall of the channel;

[forming source and drain regions coupled to ends of the first channel; and]

forming a gate adjacent to at least one of the sidewalls of the channel.

15. (Amended) The method as recited in claim 14, wherein the forming step comprises the steps of:

forming first and second semiconductor [silicon] line[s], each end of the silicon lines contacting [an end] one of the source and the drain;

forming an etch stop layer on an exposed side surface of each of the first and second semiconductor [silicon] lines;

epitaxially growing first and second semiconductor [silicon] layers on each etch stop layer;

etching away the first and second semiconductor [silicon] lines and the etch stop layers;

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill; and

etching a portion of the oxide fill to form an area that defines a gate, wherein the area that defines the gate is substantially centered between and substantially parallel to the source and the drain[; and

depositing a material to form a gate].

19. (Amended) The method as recited in claim 14 [16], further comprising the steps of:

implanting a portion of the epitaxially grown silicon layers between the gate and the source; and

implanting a portion of the epitaxially grown silicon layers between the gate and the drain.

20. (Amended) The method as recited in claim 19 [18], wherein the implanting step is in the range of 10 to 45 degrees relative to a vector perpendicular to a top surface of the epitaxially grown silicon layers.

21. (Amended) The method as recited in step 20 [14], wherein the implants are done in a series at approximately 90 degrees relative to each other.

Add the following new claims:

24. A method of forming an FET, comprising:

forming a first semiconductor layer having first and second ends and a central region that is thinner than said first and second ends, said central region having first and second side surfaces;

epitaxially growing a semiconductor channel region on at least one of said first and second side surfaces of said central region of said first semiconductor layer;

removing said central region of said first semiconductor layer;

forming a dielectric layer on exposed surfaces of said semiconductor channel region; and

forming a gate electrode on said dielectric layer.

25. The method of claim 24, wherein said semiconductor channel region is formed of a combination of Group IV elements.

26. The method of claim 24, wherein said semiconductor channel region is formed of an alloy of silicon and Group IV element.

27. The method of claim 24, wherein said semiconductor channel region is formed of a material selected from the group consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

28. The method of claim 27, wherein said step of removing said first semiconductor layer does not appreciably remove said semiconductor channel region.

29. The method of claim 28, wherein an etch stop is epitaxially grown between said first semiconductor layer and said semiconductor channel region.

30. The method of claim 24, wherein said gate electrode is formed of a material selected from the group consisting of polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium nitride.